Amendments to the Specification:

Please replace paragraph beginning on page 1, line 5 with the following amended paragraph:

The present invention relates to a flexible processing system.

Please replace paragraph beginning on page 1, line 13 with the following amended paragraph:

In response, the industry is adopting new technologies such as 802.11A, GPRS and EDGE wireless networking technologies that drive transparent connections between all computing, communications, audio and video devices. 802.11A transceivers communicate at the 5 GHz frequency and offer 100 Mbps throughput, in contrast to the 2.4 GHz frequency and the 11 Mbps throughput of 802.11B transceivers.

Please replace paragraph beginningon page 1, line 18 with the following amended paragraph:

General Packet Radio Service (GPRS) brings packet data connectivity to the Global System for Mobile Communications (GSM) market. GPRS integrates GSM and Internet Protocol (IP) technologies and is a bearer for different types of wireless data applications with bursty data, especially WAP-based information retrieval and database access. GPRS packet-switched data technology makes efficient use of radio and network resources. Session set-up is nearly instantaneous, while higher bit rates enable convenient personal and business applications. Consequently, GPRS not only makes wireless applications more usable, but also opens up a variety of new applications in personal messaging and wireless corporate intranet access.

Please replace paragraph beginning on page 2, line 14 with the following amended paragraph:

One way to increase processing power is to perform computations in parallel using hardwired, dedicated processors that are optimized for one particular radio frequency (RF) protocol. Although highly effective when geared to handle one RF protocol, this approach is relatively inflexible and cannot be easily switched to handle today's multi-mode cellular telephones that need to communicate with a plurality of RF protocols.

Please replace paragraph beginning on page 3, line 3 with the following amended paragraph:

Yet another approach uses reconfigurable logic computer architectures are computing systems that include an array of programmable logic and programmable interconnect elements. The elements can be configured and reconfigured by the end user to implement a wide range of logic

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functions and digital circuits and to implement custom algorithm-specific circuits that accelerate the execution of the algorithm. High levels of performance are achieved because the gate-level customizations made possible with FPGAs results in an extremely efficient circuit organization that uses customized data-paths and "hardwired" control structures. These circuits exhibit significant fine-grained, gate-level parallelism that is not achievable with programmable, instruction-based technologies such as microprocessors or supercomputers. This makes such architectures especially well suited to applications requiring the execution of multiple computations during the processing of a large amount of data. A basic reconfigurable system consists of two elements: a reconfigurable circuit resource of sufficient size and complexity, and a library of circuit descriptions (configurations) that can be down-loaded into the resource to configure it. The reconfigurable resource would consist of a uniform array of orthogonal logic elements (general-purpose elements with no fixed functionality) that would be capable of being configured to implement any desired digital function. The configuration library would contain the basic logic and interconnect primitives that could be used to create larger and more complex circuit descriptions. The circuit descriptions in the library could also include more complex structures such as counters, multiplexers, small memories, and even structures such as controllers, large memories and microcontroller cores. For example, U.S. Pat. No. 5,784,636 to Rupp on Jul. 21, 1998 discusses a reconfigurable processor architecture using a programmable logic structure called an Adaptive Logic Processor (ALP). The Rupp structure is similar to an extendible field programmable gate array (FPGA) and is optimized for the implementation of program specific pipeline functions, where the function may be changed any number of times during the progress of a computation. A Reconfigurable Pipeline Instruction Control (RPIC) unit is used for loading the pipeline functions into the ALP during the configuration process and coordinating the operations of the ALP with other information processing structures, such as memory, I/O devices, and arithmetic processing units. Multiple components having the Rupp reconfigurable architecture may be combined to produce high performance parallel processing systems based on the Single Instruction Multiple Data (SIMD) architecture concept.

Please replace paragraph beginning on page 5, lines 2 with the following amended paragraph:

A multi-mode wireless device on a single substrate includes an analog portion and a digital portion integrated on the single substrate. The analog portion includes a cellular radio core; and a short-range wireless transceiver core. The digital portion includes a multi-processor core with a

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master processor coupled to a router which distributes data from the radio chip to a serial-parallel array of DSP processors, each of which is connected to multiple DSP coprocessors. This arrangement allows for decoding both complex protocols at low data rates (like GPRS), simple protocols at high data rates (like 802.11A) and complex protocols at high data rates (like WCDMA), using the same hardware.

Please replace paragraph beginning on page 5, line 12 with the following amended paragraph:

Advantages of the system may include one or more of the following. A high performance, low overhead system for wireless communication system expanding the functionality and capabilities of a computer system is provided. The system effectively combines multiple components required to implement cellular radio, 802 11A and/or Bluetooth.TM. into a single integrated circuit device. The complete integration of components greatly reduces manufacturing costs. Another benefit is the fact that a single chip solution results in much lower communication overhead, in comparison to prior art multiple chip card system. The system provides for fast, easy migration of existing designs to high performance, high efficiency single chip solutions. Many elements of the LAN and WAN architecture are the same and can be re-used. For example, the Gaussian filter is used both in GSM communication and in Bluetooth communication. Similarly, the MLSE decoder and convolutional decoder are present in almost every wireless protocol, so they can be used without resource duplication. The system provides a combination of software/DSP/ASIC resources that are globally and transparently `alterable` and that can be scaled to provide vast processing power to handle the requirements of RF digital signal processing.

Please replace paragraph beginning on page 7, line 3 with the following amended paragraph:

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

Please replace paragraph beginning on page 8, line 2 with the following amended paragraph:

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to

limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

Please replace paragraph beginning on page 8, line 22 with the following amended paragraph:

The reconfigurable processor core 150 can include one or more general-purpose processors 151 such as RISC processors and these processors can support digital signal processing (DSP) capability through dual multiply-accumulate (MAC) circuits, for example. The processor core 150 includes a reconfigurable logic core 153. The reconfigurable logic core 153 can be a 'flexible' application specific integrated circuit (ASIC) block in front and possibly in between the processors 151. The reconfigurable logic core 153 can, but normally does not fetch data/instructions from memory. Rather, the reconfigurable logic core 153 gets data directly from the A/D converters to perform the initial computations.

Please replace paragraph beginning on page 9, line 8 with the following amended paragraph:

In one implementation, the reconfigurable logic core 153 is programmed as a hardcoded vector processor in front of the general purpose processor cores 151, to do the bulk of the processing and to 'parallelize' the data output. This parallel data output would then be fed simultaneously to all general purpose processor cores 151 (rather than in series) for additional DSP operation. The reconfigurable logic core 153 pre-packages the data so that the processor cores 151 working in parallel can efficiently process the RF data stream. The general-purpose processor cores 151, upon detecting that a high-speed standard is being used, select this parallel mode. The processor cores 151 also selects the ASIC preprocessor function of the reconfigurable logic core 153, which though hardcoded can still be customized on the fly by selecting one or more architecture selection switches. In one embodiment, a router 190 is used to de-correlate the incoming data such as data from 802.11 or GPRS transmitters and send the de-correlated data to the processor cores 151. Typically, data coming is 'related', so a block of, for example, 200 bits is needed to

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reconstruct the original signal. The router takes this data-word and converts the stream into parallel streams that are not time-correlated so that the processors can operate in parallel.

Please replace paragraph beginning on page 10, line 13 with the following amended paragraph:

One exemplary processor embedded in the multi-processor core 150 includes a register bank, a multiplier, a barrel shifter, an arithmetic logic unit (ALU) and a write data register. The exemplary processor can handle DSP functions by having a multiply-accumulate (MAC) unit in parallel with the ALU. Embodiments of the processor can rapidly execute multiply-accumulate (MAC) and add-compare-subtract (ACS) In another embodiment, a DSP co-processor can be provided to supplement the RISC processor cores. In these embodiments, the processor can execute instructions in either scalar or vector mode. Other parts of the exemplary processor include an instruction pipeline, a multiplexer, one or more instruction decoders, and a read data register. A program counter (PC) register addresses the memory system 170. A program counter controller serves to increment the program counter value within the program counter register as each instruction is executed and a new instruction must be fetched for the instruction pipeline. Also, when a branch instruction is executed, the target address of the branch instruction is loaded into the program counter by the program counter controller. The processor core 150 incorporates data pathways between the various functional units. The lines of the data pathways may be synchronously used for writing information into the core 150, or for reading information from the core 150. Strobe lines can be used for this purpose.

Please replace paragraph beginning on page 11, line 19 with the following amended paragraph:

Through the router 190, the multi-mode wireless communicator device 100 can detect and communicate with any wireless system it encounters at a given frequency. The router 190 performs the switch in real time through an engine that keeps track of the addresses of where the packets are going. The router 190 can send packets in parallel through two or more separate pathways. For example, if a Bluetooth.TM. connection is established, the router 190 knows which address it is looking at and will be able to immediately route packets using another connection standard. In doing this operation, the router 190 working with the RF sniffer 111 periodically scans its radio environment (`ping`) to decide on optimal transmission medium. The router 190 can send some packets in parallel through both the primary and secondary communication channel to make sure some of the packets arrive at their destinations.

Please replace paragraph beginning on page 13, line 7 with the following amended paragraph:

For voice reception, the combined signals are processed by the processor core 150 to form PCM voice samples that are subsequently converted into an analog signal and provided to an external speaker or earphone. For data reception, the processor simply transfers the data over an input/output (I/O) port During voice transmission, an off-chip microphone captures analog voice signals, digitizes the signal, and provides the digitized signal to the processor core 150. The processor core 150 codes the signal and reduces the bit-rate for transmission. The processor core 150 converts the reduced bit-rate signals to modulated signals such as I, I, Q, Q modulating signals, for example. During data transmission, the data is modulated and the modulated signals are then fed to the cellular telephone transmitter of the transmitter/receiver section.

Please replace paragraph beginning on page 13, line 17 with the following amended paragraph:

Turning now to the short-range wireless transceiver core 130, the short-range wireless transceiver core 130 contains a radio frequency (RF) modem core 132 that communicates with a link controller core 134. The processor core 150 controls the link controller core 134. In one embodiment, the RF modem core 132 has a direct-conversion radio architecture with integrated VCO and frequency synthesizer. The RF-unit 132 includes an RF receiver connected to an analog-digital converter (ADC), which in turn is connected to a modem 116 performing digital modulation, channel filtering, AFC, symbol timing recovery, and bit slicing operations. For transmission, the modem is connected to a digital to analog converter (DAC) that in turn drives an RF transmitter.

Please replace paragraph beginning on page 14, line 3 with the following amended paragraph:

The link controller core 134 provides link control function and can be implemented in hardware or in firmware. One embodiment of the core 134 is compliant with the Bluetooth.TM. specification and processes Bluetooth.TM. packet types. For header creation, the link controller core 134 performs a header error check, scrambles the header to randomize the data and to minimize DC bias, and performs forward error correction (FEC) encoding to reduce the chances of getting corrupted information. The payload is passed through a cyclic redundancy check (CRC), encrypted/scrambled and FEC-encoded. The FEC encoded data is then inserted into the header.

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Please replace paragraph beginning on page 14, line 21 with the following amended paragraph:

When the multi-mode wireless communicator device 100 is in the cellular telephone connection mode, the short-range wireless transceiver core 130 is powered down to save power. Unused sections of the chip are also powered down to save power. Many other battery-power saving features are incorporated, and in particular, the cellular radio core 110 when in the standby mode can be powered down for most of the time and only wake up at predetermined instances to read messages transmitted by cellular telephone base stations in the radio's allocated paging time slot.

Please replace paragraph beginning on page 15, line 22 with the following amended paragraph:

The router 190 can send packets in parallel through the separate pathways of cellular or Bluetooth.TM.. For example, if a Bluetooth.TM. connection is established, the router 190 knows which address it is looking at and will be able to immediately route packets using another connection standard. In doing this operation, the router 190 pings its environment to decide on optimal transmission medium. If the signal reception is poor for both pathways, the router 190 can send some packets in parallel through both the primary and secondary communication channel (cellular and/or Bluetooth.TM.) to make sure some of the packets arrive at their destinations. However, if the signal strength is adequate, the router 190 prefers the Bluetooth.TM. mode to minimize the number of subscribers using the capacity-limited and more expensive cellular system at any give time. Only a small percentage of the device 100, those that are temporarily outside the Bluetooth coverage, represents a potential load on the capacity of the cellular system, so that the number of mobile users can be many times greater than the capacity of the cellular system alone could support.

Please replace paragraph beginning on page 16, line 13 with the following amended paragraph:

FIG. 1B is a block diagram of an exemplary multi-processor system. A master processor 302 interfaces to a host system that can include RF circuitry. The master processor 302 in turn communicates with a programmable block 304, an application specific processor block 306 and a router block 308. The router block 308 communicates with one or more processing units, each including a processor and one or more digital signal processors (DSPs). In the embodiment of FIG. 1B, processor 310 communicates with one or more DSPs 312, processor 320 communicates with one or more DSPs 322, and processor 330 communicates with one or more DSPs 332. As discussed above, the router block 308 is used to de-correlate the incoming data such as data from

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802.11 or GPRS transmitters and send the de-correlated data to the processors 310, 320 and 330. Typically, data coming is 'related', so a block of data is needed to reconstruct the original signal. The router block 308 takes this data-word and converts the stream into parallel streams that are not time-correlated so that the processors can operate in parallel.

Please replace paragraph beginning on page 17, line 3 with the following amended paragraph:

Each DSP processor is a simple, small RISC processor that controls the DSP functions in a high level language such as C. The master processor 302 is a RISC processor which does all the flow control. The DSP subunits 312, 322 and 332 are small coprocessors that perform mathematical functions such as multiply-accumulate and add-compare-select.

Please replace paragraph beginning on page 17, line 8 with the following amended paragraph:

The system of FIG. 2 supports 4 dimensional computing capability. In Dimension 1, each processor is doing a specific separate task. For example, one processor processes Bluetooth signal while another processor handles GPS processing. In Dimension 2, each processor is doing tasks in series with the other processors. For example, one processor performs GPRS equalization, moves the data to the next processor which does convolutional decoding, moving the data to the next processor which does vocoder decoding. This way slow, complicated functions like GPRS can be performed.

Please replace paragraph beginning on page 18, line 1 with the following amended paragraph:

FIG. 2 illustrates an exemplary computer system 200 with the wireless communication device 100. The computer system 200 is preferably housed in a small, rectangular portable enclosure. Referring now to FIG. 2, a general purpose architecture for entering information into the data management by writing or speaking to the computer system is illustrated A processor 220 or central processing unit (CPU) provides the processing capability. The processor 220 can be a reduced instruction set computer (RISC) processor or a complex instruction set computer (CISC) processor. In one embodiment, the processor 220 is a low power CPU such as the MC68328V DragonBall device available from Motorola Inc.

Please replace paragraph beginning on page 19, line 19 with the following amended paragraph:

The processor 220 drives an internal bus 226. Through the bus 226, the computer system can access data from the ROM 221 or RAM 222, or can acquire I/O information such as visual

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information via a charged coupled device (CCD) 228. The CCD unit 228 is further connected to a lens assembly (not shown) for receiving and focusing light beams to the CCD for digitization. Images scanned via the CCD unit 228 can be compressed and transmitted via a suitable network such as the Internet, through Bluetooth channel, cellular telephone channels or via facsimile to a remote site.

Please replace paragraph beginning on page 20, line 17 with the following amended paragraph:

The processor 220 of the preferred embodiment accepts handwritings as an input medium from the user. A digitizer 234, a pen 233, and a display LCD panel 235 are provided to capture the handwriting. Preferably, the digitizer 234 has a character input region and a numeral input region that are adapted to capture the user's handwritings on words and numbers, respectively. The LCD panel 235 has a viewing screen exposed along one of the planar sides of the enclosure are provided. The assembly combination of the digitizer 234, the pen 233 and the LCD panel 235 serves as an input/output device. When operating as an output device, the screen 235 displays computer-generated images developed by the CPU 220. The LCD panel 235 also provides visual feedback to the user when one or more application software execute. When operating as an input device, the digitizer 234 senses the position of the tip of the stylus or pen 233 on the viewing screen 235 and provides this information to the computer's processor 220. In addition to the vector information, the present invention contemplates that display assemblies capable of sensing the pressure of the stylus on the screen can be used to provide further information to the CPU 220.

Please replace paragraph beginning on page 21, line 9 with the following amended paragraph:

The CPU 220 accepts pen strokes from the user using the stylus or pen 233 that is positioned over the digitizer 234. As the user "writes," the position of the pen 233 is sensed by the digitizer 234 via an electromagnetic field as the user writes information to the computer system. The digitizer 234 converts the position information to graphic data. For example, graphical images can be input into the pen-based computer by merely moving the stylus over the surface of the screen. As the CPU 220 senses the position and movement of the stylus, it generates a corresponding image on the screen to create the illusion that the pen or stylus is drawing the image directly upon the screen. The data on the position and movement of the stylus is also provided to handwriting recognition software, which is stored in the ROM 221 and/or the RAM

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222. The handwriting recognizer suitably converts the written instructions from the user into text data suitable for saving time and expense information. The process of converting the pen strokes into equivalent characters and/or drawing vectors using the handwriting recognizer is described below.

Please replace paragraph beginning on page 22, line 1 with the following amended paragraph:

The computer system is also connected to one or more input/output (I/O) ports 242 which allow the CPU 220 to communicate with other computers. Each of the I/O ports 242 may be a parallel port, a serial port, a universal serial bus (USB) port, a Firewire port, or alternatively a proprietary port to enable the computer system to dock with the host computer. In the event that the I/O port 242 is housed in a docking port, after docking, the I/O ports 242 and software located on a host computer (not shown) support an automatic synchronization of data between the computer system and the host computer. During operation, the synchronization software runs in the background mode on the host computer and listens for a synchronization request or command from the computer system 200 of the present invention. Changes made on the computer system and the host computer will be reflected on both systems after synchronization. Preferably, the synchronization software only synchronizes the portions of the files that have been modified to reduce the updating times. The I/O port 242 is preferably a high speed serial port such as an RS-232 port, a Universal Serial Bus, or a Fibre Channel for cost reasons, but can also be a parallel port for higher data transfer rate.

Please replace paragraph beginning on page 22, line 16 with the following amended paragraph:

One or more portable computers 200 can be dispersed in nearby cell regions and communicate with a cellular mobile support station (MSS) as well as a Bluetooth station. The cellular and Bluetooth stations relay the messages via stations positioned on a global basis to ensure that the user is connected to the network, regardless of his or her reference to home. The stations are eventually connected to the Internet, which is a super-network, or a network of networks, interconnecting a number of computers together using predefined protocols to tell the computers how to locate and exchange data with one another. The primary elements of the Internet are host computers that are linked by a backbone telecommunications network and communicate using one or more protocols. The most fundamental of Internet protocols is called Transmission Control Protocol/Internet Protocol (TCP/IP), which is essentially an envelope where data resides.

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The TCP protocol tells computers what is in the packet, and the IP protocol tells computers where to send the packet. The IP transmits blocks of data called datagrams from sources to destinations throughout the Internet. As packets of information travel across the Internet, routers throughout the network check the addresses of data packages and determine the best route to send them to their destinations. Furthermore, packets of information are detoured around non-operative computers if necessary until the information finds its way to the proper destination.

Please replace paragraph beginning on page 23, line 19 with the following amended paragraph:

The browser commonly features a graphical user interface with icons and menus across the top along with a field to supply the URL for retrieval purposes. Navigational buttons guide the users through cyberspace in a linear manner, either one page forward or backward at a time. Pull down menus provide a history of sites accessed so that the user can revisit previous pages. A stop button is typically provided to cancel the loading of a page. To preserve favorite sites, a bookmark is provided to hold the user's favorite URLs in a list such as a directory tree. Furthermore, the browser typically provides a temporary cache on the data storage device or in RAM. The cache allows a more efficient Internet access as it saves bandwidth and improves access performance significantly. The browser also interprets HyperText Markup Language (HTML) which allows web site creators to specify a display format accessible by HTML compatible browsers.

Please replace paragraph beginning on page 25, line 11 with the following amended paragraph:

The system enables easy synchronization and mobility during a cordless connection regardless of distance. The system opens up possibilities for establishing quick, temporary (ad-hoc) connections with colleagues, friends, or office networks. Appliances using the device 100 are easy to use since they can be set to automatically find and contact each other when within range. For example, a user is in his or her office and browses a web site on a portable computer through a wired local area network cable such as an Ethernet cable. Then the user walks to a nearby cubicle. As the user disconnects, the device 100 initiates a short-range connection using a Bluetooth.TM. connection. When the user drives from his or her office to an off-site meeting, the Bluetooth.TM. connection is replaced with cellular telephone connection. Further, when the multi-mode wireless communicator device 100 is in the cellular telephone connection mode, the

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short-range wireless transceiver core 130 is powered down to save power. Unused sections of the chip are also powered down to save power.

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